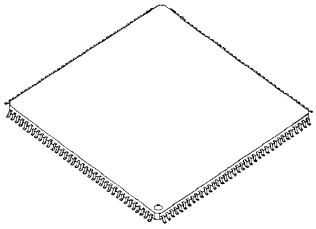
Preliminary

16COM x 100SEG 1/16 Duty BITMAP LCD Driver

■ GENERAL DESCRIPTION

The NJU6573 is a 16-common x 100-segment bitmap LCD driver to display graphics or characters. It incorporates 16 common driver circuits and 100 segment driver circuits. The NJU6573 can display a 16 x 100 dots graphic or 2-line by 20-character (5 x 7 dots per character).
In addition, the NJU6573's useful functions meet a wide range of applications.

PACKAGE OUTLINE

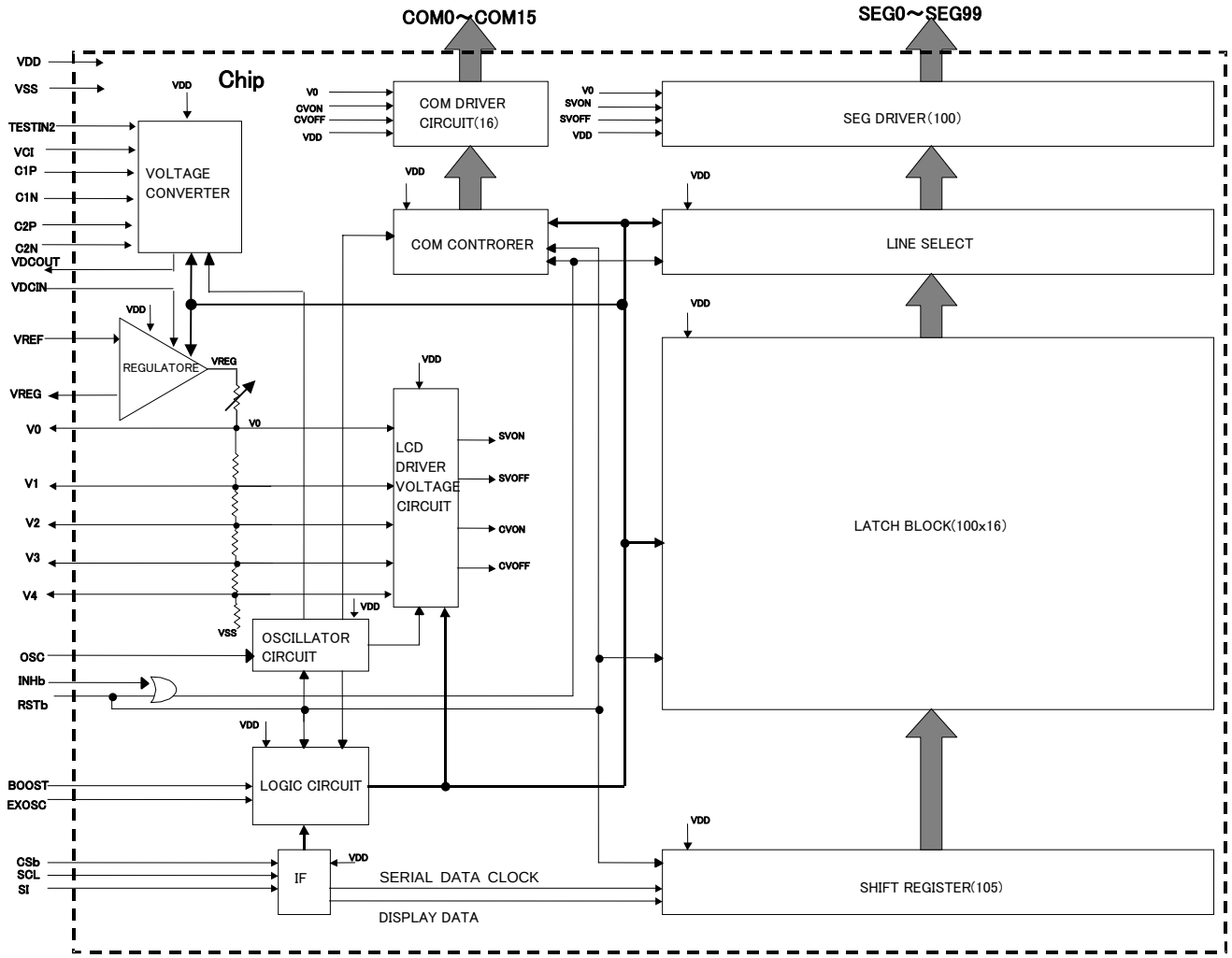


NJU6573

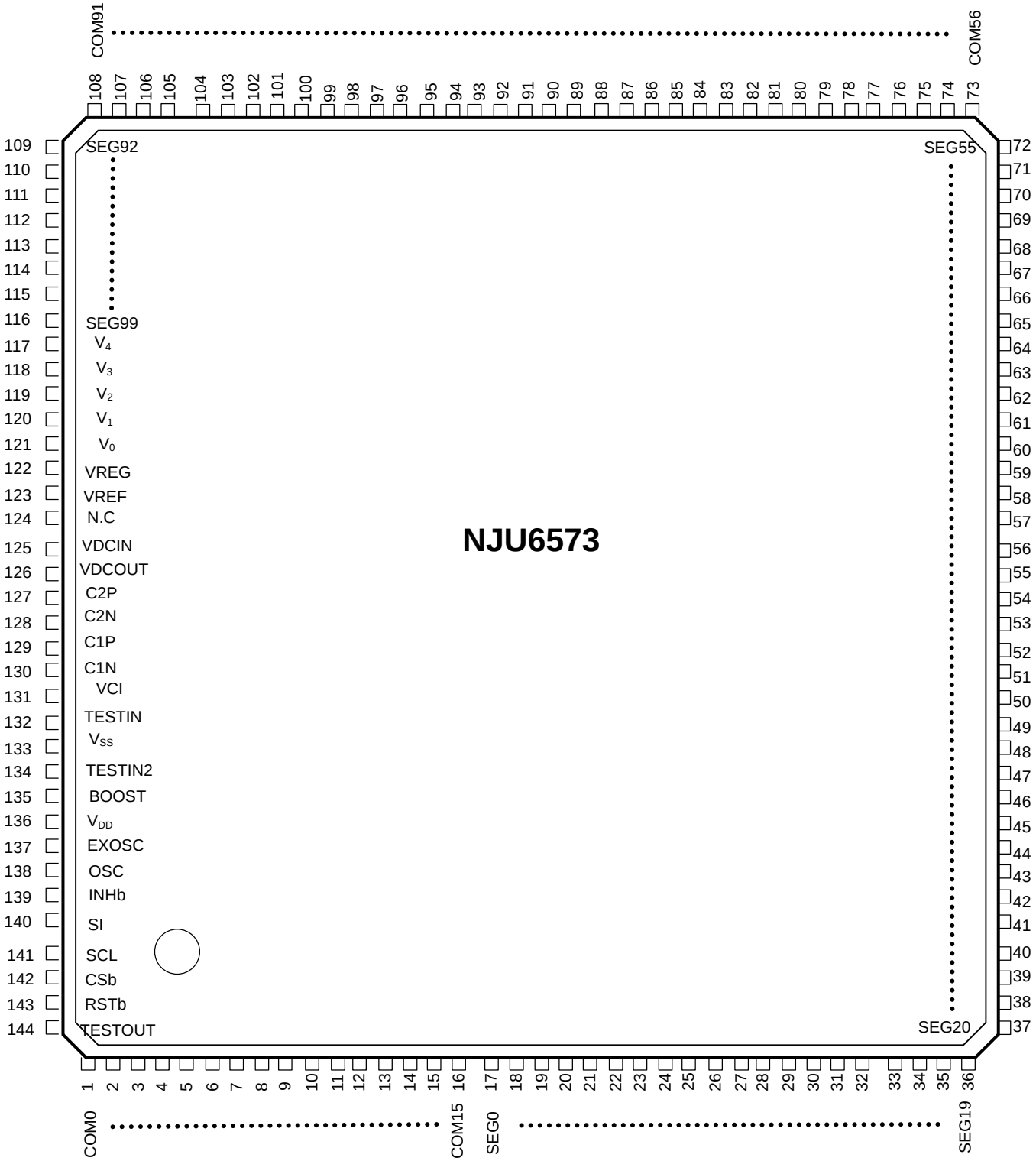
■ FEATURES

LCD driving circuit : 16-common and 100-segment
Bias Ratio : 1/5 bias
Serial Data Transfer : Shift clock max. 2MHz
Oscillator : CR oscillation with external resistor and capacitor, or external oscillation signal input.
Programmable Contrast Control:16-steps Electrical Variable Resister (EVR)
Voltage Tripler and bleeder resistance on-chip.
Operating Voltage : V_{DD}=2.4~3.6V
C-MOS Technology : Substrate : P
Package : LQFP144 20.0mm x 20.0mm t=1.7mm(Max)
0.5mm pitch

■ BLOCK DIAGRAM



■ PAD LOCATION



■ TERMINAL DISCRIPTION

<table>
<tr><th>No.</th><th>Pad Name</th><th>Function</th></tr>
<tr><td>136</td><td>VDD</td><td>Power Supply: (2.4V-3.6V)</td></tr>
<tr><td>131
122
123</td><td>VCI
VREG
VREF</td><td>Booster voltage input terminal(MAX:3.3V)
Voltage Regulator Output
Regulator base voltage input terminal for VREG output (MAX:3.3V)</td></tr>
<tr><td>139</td><td>INHb</td><td>Display ON or OFF “High”=Display ON, “Low”=Display OFF,</td></tr>
<tr><td>125</td><td>VDCIN</td><td>Voltage Regulator Input</td></tr>
<tr><td>126</td><td>VDCOUT</td><td>Booster voltage output terminal (Internal Booster Circuit Output Terminal)</td></tr>
<tr><td>121
120
119
118
117</td><td>V0
V1
V2
V3
V4</td><td>Bias
$V0 \geq V1 \geq V2 \geq V3 \geq V4 \geq V_{SS}$</td></tr>
<tr><td>133</td><td>V_{SS}</td><td>GND Terminal V_{SS} =0V</td></tr>
<tr><td>129
130
127
128</td><td>C1P
C1N
C2P
C2N</td><td>Capacitor Connect Terminal for Voltage Booster</td></tr>
<tr><td>143</td><td>RSTb</td><td>Reset
When RSTb is “Low”, Latch Circuit is Reset.</td></tr>
<tr><td>142</td><td>CSb</td><td>Chip Select
When CSb is “Low”, Data can be read in.</td></tr>
<tr><td>140</td><td>SI</td><td>Serial Data Input Terminal</td></tr>
<tr><td>141</td><td>SCL</td><td>Serial Clock Input Terminal (Max: 2MHz)</td></tr>
<tr><td>138
137</td><td>OSC
EXOSC</td><td>OSC: External Resistor and Capacitor Connect Terminal for CR Oscillation, or External Clock Input Terminal.
EXOSC: “High”=External Clock Input, “Low”=CR Connect,</td></tr>
<tr><td>1-16</td><td>COM0-COM15</td><td>Common Driver Outputs</td></tr>
<tr><td>17-116</td><td>SEG0-SEG99</td><td>Segment Driver Outputs</td></tr>
<tr><td>135</td><td>BOOST</td><td>Voltage Booster ON or OFF
“High”=Voltage Booster ON, “Low”=Voltage Booster OFF,
<table>
<tr><th>BOOST</th><th>Internal Booster Circuit</th><th>Internal Regulator</th></tr>
<tr><td>L</td><td>OFF</td><td>OFF</td></tr>
<tr><td>H</td><td>ON</td><td>ON</td></tr>
</table></td></tr>
<tr><td>132</td><td>TESTIN</td><td>Test Terminal (Keep TESTIN-Vss short)</td></tr>
<tr><td>134</td><td>TESTIN2</td><td>Test2 Terminal (Keep TESTIN2-Vss short)</td></tr>
<tr><td>144</td><td>TESTOUT</td><td>Test Out Terminal（There is open Terminal electrically）</td></tr>
<tr><td>124</td><td>N.C.</td><td>There is open Terminal electrically</td></tr>
</table>

■ FUNCTION DESCRIPTION

(1) Shift Resister
105 bits resister

(2) Latch Circuit
Data stored in display data register is assigned to the corresponding SEG/port.

(3) Segment Driver
Basing on display data, segment drivers output LCD SEG driving signal.

(4) Common Driver
Common drivers output LCD COM driving signal.

(5) Voltage Booster
NJU6573 with a built-in Voltage Booster. The internal voltage booster generates up to 3xVCI voltage(Input:VCI Terminal, Output: VDCOUT Terminal). The boost voltage VDCOUT must not exceed 10.0V(VCIx3≤ 10V), otherwise the voltage stress may case a permanent damage to the LSI. When using the internal LCD power supply, connect the VDCOUT and the VDCIN.
The VREF voltage is tripled to obtain the VREG voltage.(VREFx3=VREG)

(5) Bleeder Resistance

Each LCD driving voltage (V1, V2, V3, V4) is LCD driving high voltage input to the V_0 Terminal, generated by the E.V.R and high impedance bleeder resistance.

LCD driving voltage generation circuit generates LCD driving bias voltages V0, V1, V2, V3 and V4. V_{REG}, V0, V1, V2, V3 and V4 terminals requires external capacitors for bias voltage stabilization for display quality. These values of capacitors should be fixed in accordance with evaluation in the application.

LCD Driving Voltage vs Duty Ratio

Power supply	Duty Ratio	1/16
	Bias	1/5
V_{LCD}		V_0- V_{SS}

V_{LCD} is the maximum amplitude for LCD driving voltage.

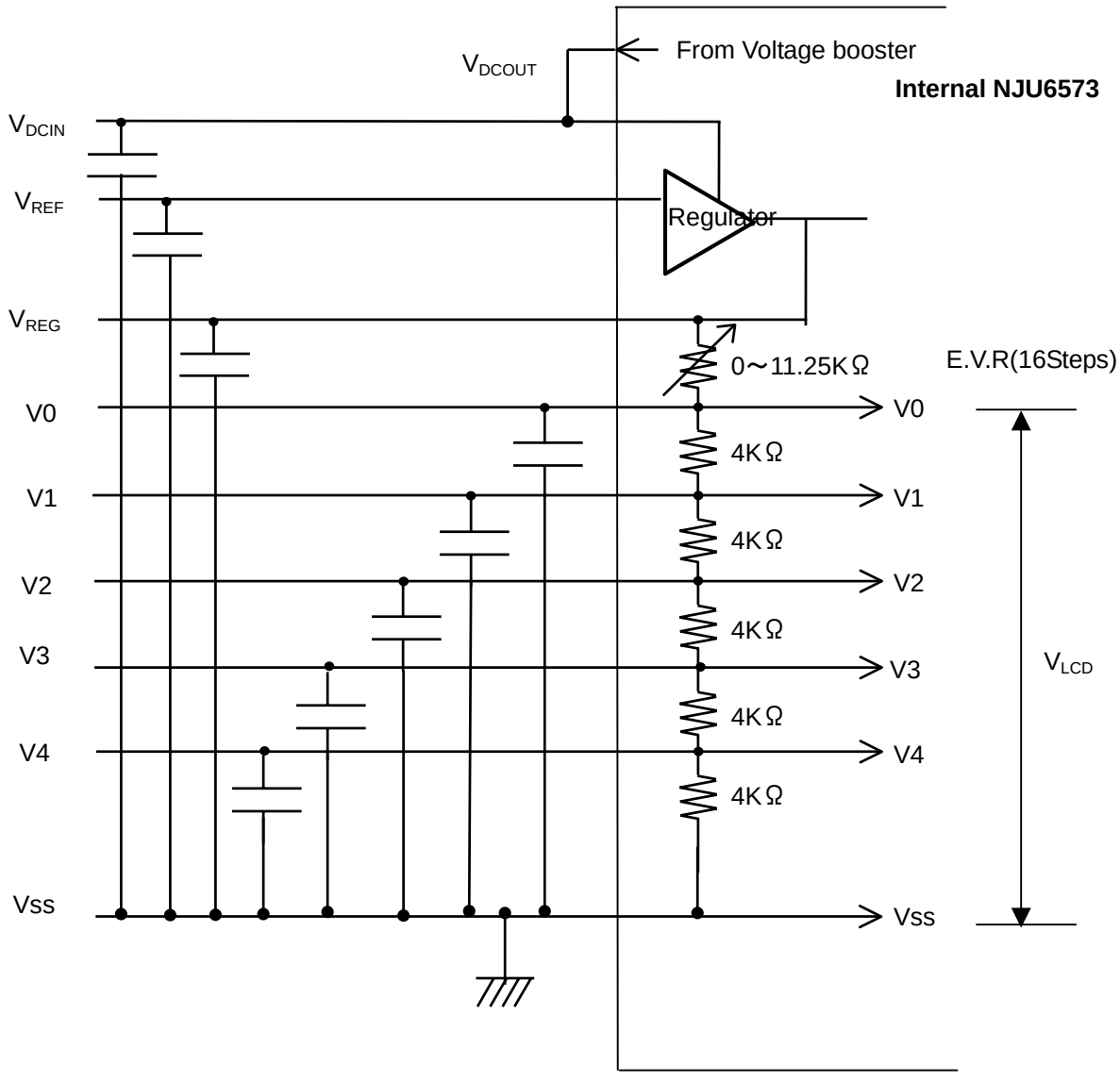


Fig Bleeder Resistance

(6) Oscillator circuit

The oscillator consists of an external capacitor and an resistor. It generates clock signal for LCD driving. When use external clock, input the clock signal to OSC.(EXOSC Terminal is “High” when use external clock)

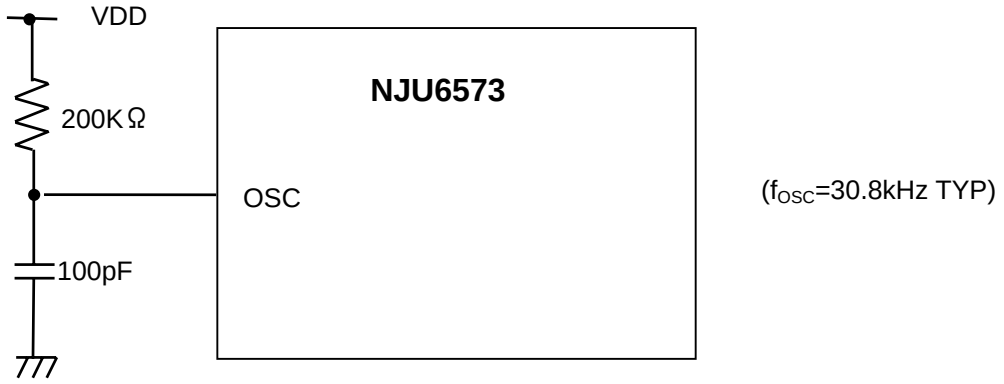


Fig OSC Circuit

(6-1) Relation between Oscillation frequency and Frame frequency

Frame frequency = fosc / 384

Set the oscillation frequency to obtain the frame frequency.

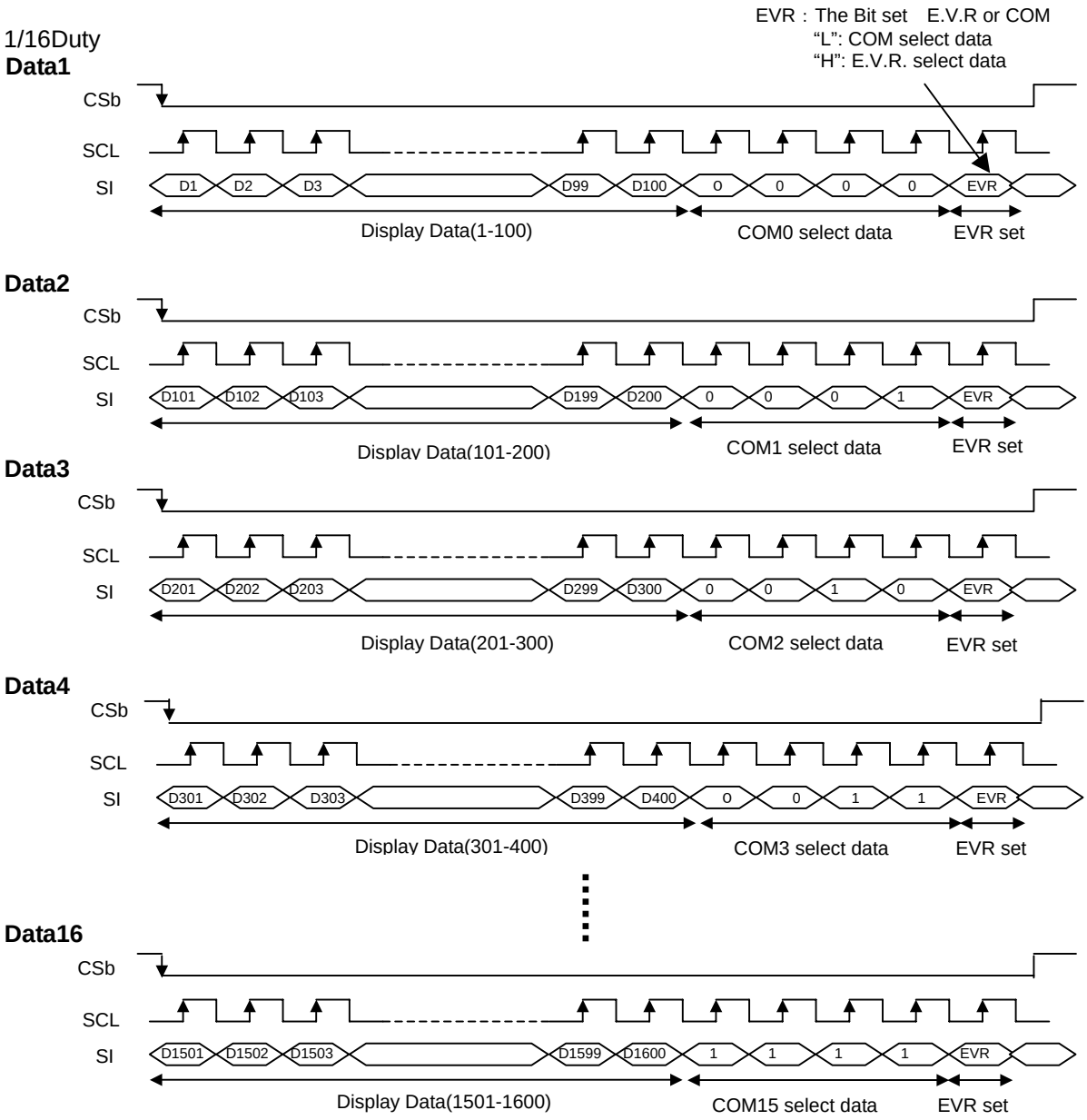
(7) Input Data Format and Timing

Data format is shown below.

When the CSb terminal goes to “L” at SCL terminal “H”, I/F is data input. Data fetched at SCL rising edge.

In case of entering less then 105-bit data(Display Data:100bit, COM select data:4bit,E.V.R set data:1bit), Malfunction. In case of entering over then 105-bit data, valid data is last 105-bit data.

(7-1) 1/16Duty



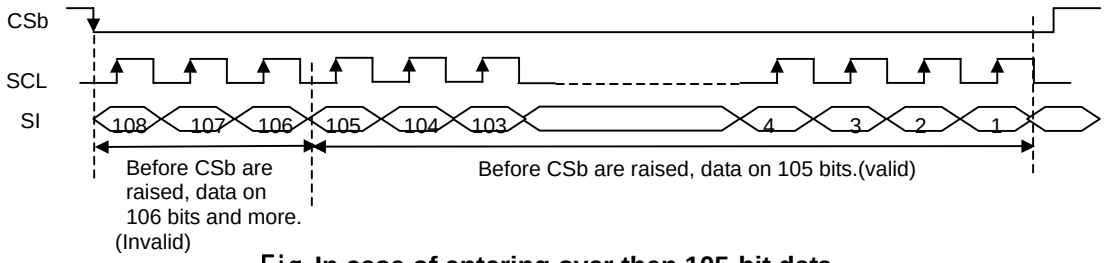


Fig In case of entering over then 105-bit data

(7-2) Voltage Booster Circuit Select (BOOST terminal)
Voltage Booster ON or OFF

BOOST	H	L
Voltage Booster Circuit	ON	OFF
Regulator Circuit	ON	OFF
VLCD operation supply	Internal Booster Circuit using	External VLCD power supply Input

(7-3) Display OFF (INHb)
Display ON or OFF

INHb	H	L
Display	ON	OFF
SEG, COM Output	LCD wave form Output	VSS

(7-4) Reset(RSTb)

NJU6573 is initialized to the following values:

- Electrical Voltage Resistor: “0000”
- Display data latch status: All data “0”

During Reset status

- Stop the Oscillation circuit
- Segment and Common drivers output VSS level.

NJU6573 does not always require reset operation.
The reset operation is recommended to initialize internal registers.

(7-5) Supply Voltage Sequence Example

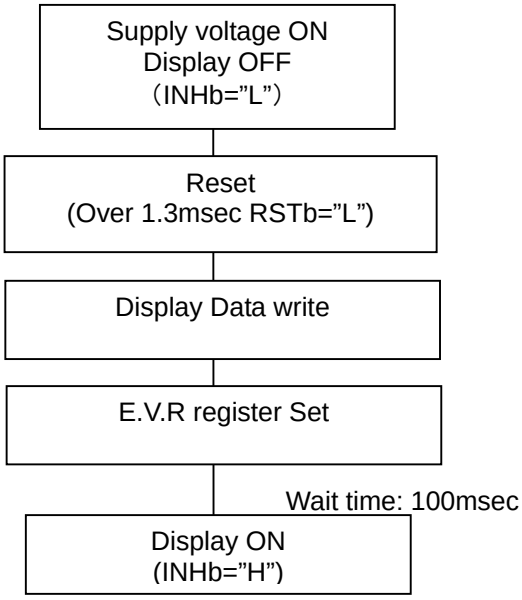


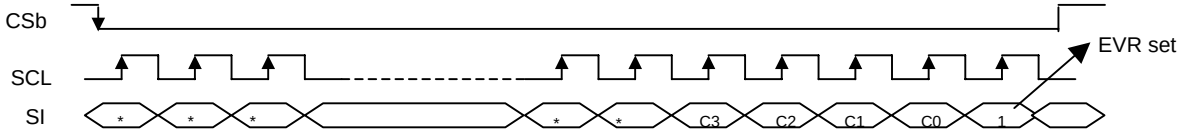
Fig Supply Voltage Sequence Example

(8) Instructions

The **NJU6573** incorporates E.V.R register(high). Instruction code as show below.

Table. Table of Instructions

Instruction	Explanation
Electrical Voltage Resistor	When the CSb terminal rising edge eve one bit is High, Data fetched at SCL rising edge. In case of entering less then 2-5bit data valid.



*: Even only 5 clock can set E.V.R if the last bit is "1".

＊：Don't care

Contrast Control instruction which adjusts the contrast of the LCD is executed when the code "1" is written into EVR and the codes of C3 to C0 are written into 2 to 5bit as shown below.

The contrast of LCD can be adjusted one of 16 voltage-stages by setting this 4-bit register.

See below "how to adjust the Contrast of LCD".

Set the binary code "1,1,1,1" when contrast adjustment is unused.

C3	C2	C1	C0	VLCD voltage (Spec)	Ex.) VLCD voltage by VOUT=8.4V
0	0	0	0	VOUT x 0.640	5.376
0	0	0	1	VOUT x 0.656	5.508
0	0	1	0	VOUT x 0.672	5.647
0	0	1	1	VOUT x 0.690	5.793
0	1	0	0	VOUT x 0.708	5.947
0	1	0	1	VOUT x 0.727	6.109
0	1	1	0	VOUT x 0.748	6.280
0	1	1	1	VOUT x 0.769	6.462
1	0	0	0	VOUT x 0.792	6.653
1	0	0	1	VOUT x 0.816	6.857
1	0	1	0	VOUT x 0.842	7.074
1	0	1	1	VOUT x 0.870	7.304
1	1	0	0	VOUT x 0.899	7.551
1	1	0	1	VOUT x 0.930	7.814
1	1	1	0	VOUT x 0.964	8.096
1	1	1	1	VOUT x 1.000	8.400

VLCD=VREG x 20 / (31.25-0.75 x M)

M: Contrast control resistor = 0-15

- Input Data v.s output

	COM0	COM1	COM2	COM3	→	COM12	COM13	COM14	COM15
COM	0000	0001	0010	0011	→	1100	1101	1110	1111
SEG0	D1	D101	D201	D301	→	D1201	D1301	D1401	D1501
SEG1	D2	D102	D202	D302	→	D1202	D1302	D1402	D1502
SEG2	D3	D103	D203	D303	→	D1203	D1303	D1403	D1503
SEG3	D4	D104	D204	D304	→	D1204	D1304	D1404	D1504
SEG4	D5	D105	D205	D305	→	D1205	D1305	D1405	D1505
SEG5	D6	D106	D206	D306	→	D1206	D1306	D1406	D1506
SEG6	D7	D107	D207	D307	→	D1207	D1307	D1407	D1507
SEG7	D8	D108	D208	D308	→	D1208	D1308	D1408	D1508
SEG8	D9	D109	D209	D309	→	D1209	D1309	D1409	D1509
SEG9	D10	D110	D210	D310	→	D1210	D1310	D1410	D1510
↓	↓	↓	↓	↓	→	↓	↓	↓	↓
SEG89	D91	D191	D291	D391	→	D1291	D1391	D1491	D1591
SEG90	D92	D192	D292	D392	→	D1292	D1392	D1492	D1592
SEG91	D93	D193	D293	D393	→	D1293	D1393	D1493	D1593
SEG92	D94	D194	D294	D394	→	D1294	D1394	D1494	D1594
SEG93	D95	D195	D295	D395	→	D1295	D1395	D1495	D1595
SEG95	D96	D196	D296	D396	→	D1296	D1396	D1496	D1596
SEG96	D97	D197	D297	D397	→	D1297	D1397	D1497	D1597
SEG97	D98	D198	D298	D398	→	D1298	D1398	D1498	D1598
SEG98	D99	D199	D299	D399	→	D1299	D1399	D1499	D1599
SEG99	D100	D200	D300	D400	→	D1300	D1400	D1500	D1600

■ ABSOLUTE MAXIMAM RATINGS

(V_{SS}=0V, Ta=25°C)

PARAMETER	SYMBOL	RATINGS	UNIT	CONDITIONS
Supply Voltage 1	V_{DD},V_{REF}	-0.3 ~ +7.0	V	
Supply Voltage 2	V_{CI}	-0.3 ~ +10.5	V	V_{CI} Terminal Note-4)
Supply Voltage 3	V_{DCIN}, V_0 V_1~V_4,V_{REG}	-0.3 ~ +10.5	V	V_{DCIN}, V_0, V_1~V_4 ,V_{REG} Terminal
Input Voltage	V_t	-0.3 ~ V_{DD}+0.3	V	INHb, CSb, SCL, SI, RSTb, OSC, BOOST EXOSC,TESTIN,TEST2, applicable.
Operating Temp.	Topr	-40 ~ +105	°C	
Storage Temp.	Tstg	-55 ~ +125	°C	
Dissipation Power	P_D	1000	mW	The power dissipation is value mounted on 4 layer glass epoxy board in size 76.2mm x 114.3mm x 1.6tmm

Note-1) Do not exceed the absolute maximum ratings, otherwise the stress may cause a permanent damage to the IC. It is also recommended that the IC be used within the range specified in the DC electrical characteristics, or the electrical stress may cause mulfunctions and impact on the reliability.

Note-2) To stabilize the LSI operation, place decoupling capacitors between V_{DD}-V_{SS}, V_{CI}-V_{SS} and between V_{DCIN}-V_{SS}.

Note-3) All voltages are relative to V_{SS} = 0V reference.The following relationship shall be maintained.
$V_{DCIN} \geq V_0 \geq V_{DD} > V_{SS}$, and V_{SS} =0V

Note-4) When voltage booster circuit, need condition of 10V ≥ VCIx3.

ELECTRICAL CHARACTERISTICS

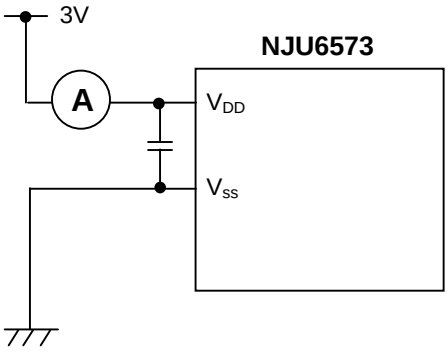
• DC characteristics (V_{DD}=2.4 to 3.6V, V_{SS}=0V, Ta=-40 to +105°C)

PARAMETER	SYMBOL	Terminal	CONDITIONS	MIN	TYP	MAX	UNIT	Note
Power Supply 1	V_{DD}	V_{DD}		2.4	-	3.6	V	
Power Supply 2	V_{CI}	V_{CI}		2.4	-	3.3	V	5
Power Supply 3	V_{DCIN}	V_{DCIN}		3.6	-	10.0		6
Input voltage 1	V_{IH1}	CSb, SCL, SI, RSTb, OSC,BOOST INHb, EXOSC		0.8 V_{DD}	-	V_{DD}	V	
	V_{IL1}			V_{SS}	-	0.2 V_{DD}	V	
Driver-on(COM) Resistance	R_{COM}	COM0-COM15	±Id=1μA(COM Terminal) V_O=V_0,V_{SS}, V_1,V_4	-	-	20	kOhm	7
Driver-on(SEG) Resistance	R_{SEG}	SEG0-SEG99	±Id=1μA(SEG Terminal) V_O=V_0,V_{SS}, V_2,V_3	-	-	20	kOhm	7
Input leakage current	I_{LI}	CSb, SCL, RSTb, INHb, BOOST, EXOSC	V_{IN}=0~V_{DD}	-1.0	-	1.0	μA	
Operating Current	I_{DD1}	V_{DD}	V_{DD}=V_{CI}=3V, V_{REF}=2.7V, f_{osc}=30.8kHz, Checker Display ON, Booster ON, Ta=25°C E.V.R: "1111" SEG/COM open V_{DCOUT}/V_{DCIN} connect	-	30	50	μA	8
	I_{CI}	V_{CI}		-	1.5	2.0	mA	
	I_{DD1}	V_{DD}	f_{OSC}=184.8kHz Other condition same as I_{DD1}	-	90	150	μA	8
	I_{CI}	V_{CI}		-	1.7	2.2	mA	
LCD operating voltage	V_0	V_0	V_{REG} =8.0V E.V.R: "1111"	7.8	-	8.0	V	
	V_1	V_1		6.2	6.4	6.6		
	V_2	V_2		4.6	4.8	5.0		
	V_3	V_3		3.0	3.2	3.4		
	V_4	V_4		1.4	1.6	1.8		
Bleeder resistance RB=V_0/I_B RB: Bleeder resistance 5 IB: Bleeder resistance Current	R_B	V_{REG}	V_{REG} =8.0V E.V.R: "1111", Ta=25°C	14.0	20.0	26.0	kOhm	
Booster output voltage	V_{OUT}	V_{DCOUT}	V_{CI}=3.3V, Ta=25°C f_{OSC}=30.8k-184.8kHz, BoosterON(COM/SEGopen) V_{DCOUT} between V_{DCIN} connect	9.0	9.5	-	V	
OSC Frequency	f_{OSC}	OSC	V_{DD} =3V, Ta=25°C, R_{OSC}= 200kOhm C_{OSC}= 100pF	25.3	30.8	36.3	kHz	
			R_{OSC}= 30kOhm Other condition same as f_{OSC}	151.8	184.8	217.8		
External clock Operating Frequency	f_{CP}	OSC	External input	25.3	-	217.8	kHz	
Operate Frame Frequency range	Fr	COM		66	-	566	Hz	9
V_{REF} input voltage	V_{REF}	V_{REF}		1.0	-	V_{DD}	V	
Regulator output voltage	V_{REG}	V_{REG}	V_{DCIN} =10V, V_{REF}=3V, (COM/SEG open)	V_{REF} x 3 x 0.98	V_{REF} x 3	V_{REF} x 3 x 1.02	V	
Dropout Voltage	Delta VIO	V_{DCIN}-V_{REG}	V_{DCIN}=9V, V_{REF}=3.6V, I_O=-200μA	-	0.05	0.10	V	
V_{DCIN} Current	I_{OUT}	V_{DCIN}	V_{DCIN}=9.0V, V_{REF}=2.7V E.V.R: "1111", INHb=0 Ta=25°C (COM/SEG open)	-	0.5	0.8	mA	

Note-5) When voltage booster circuit using, need condition of $V_{DCOUT} \leq 10V$

Note-6) Condition of V_{DCIN} Voltage: $10V \geq V_{DCIN} \geq V_{REF} \times 3 + 0.6$

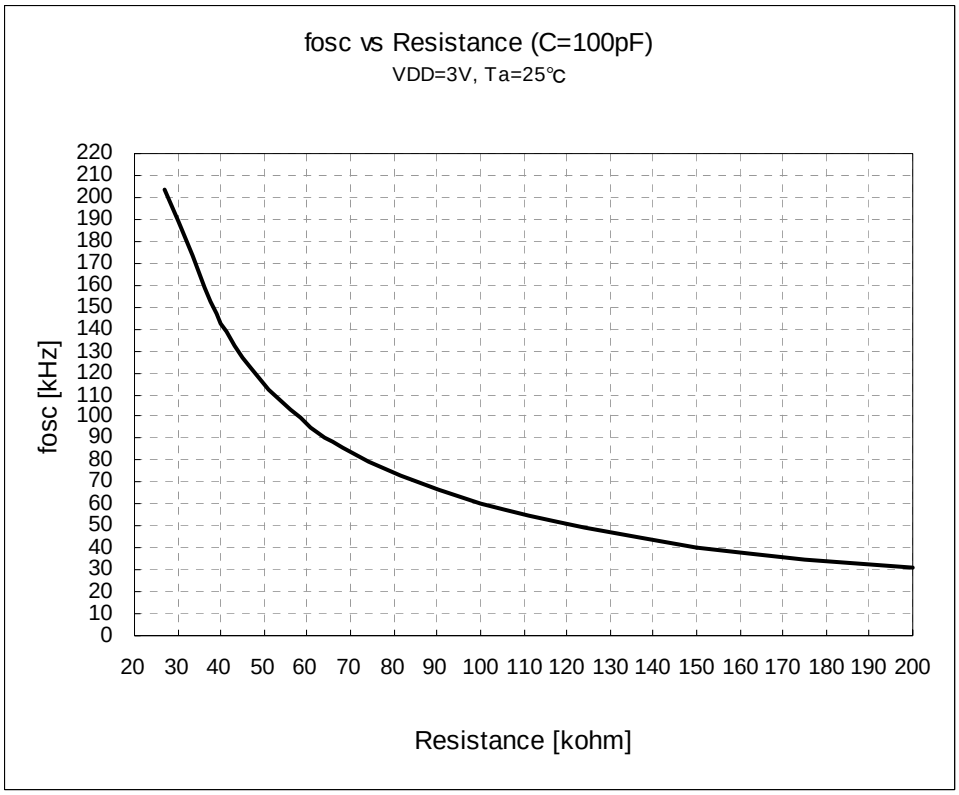
Note-7) Driver-On resistance (R_{SEG}/R_{COM}) is measured from V_0, V_{SS}, V_1 , V_2 , V_3 or V_4 terminal to each SEG/COM terminal when Id current flows through COM/SEG terminals.



Note-8) If input voltage is outside of the spec, when operating current increase. Input level must be condition “H” or “L”. This mesurement condition is SI terminal between VDD short.

Note-9) Frame frequency vs OSC is as the show relation between oscillation frequency and Frame frequency page7.

Example characteristic)
Condition
C=100[pF]
R=from 27k[ohm] to 200k[ohm]
Temperature=25[°C]
The following graph is the data of example sample, so without guarantee.

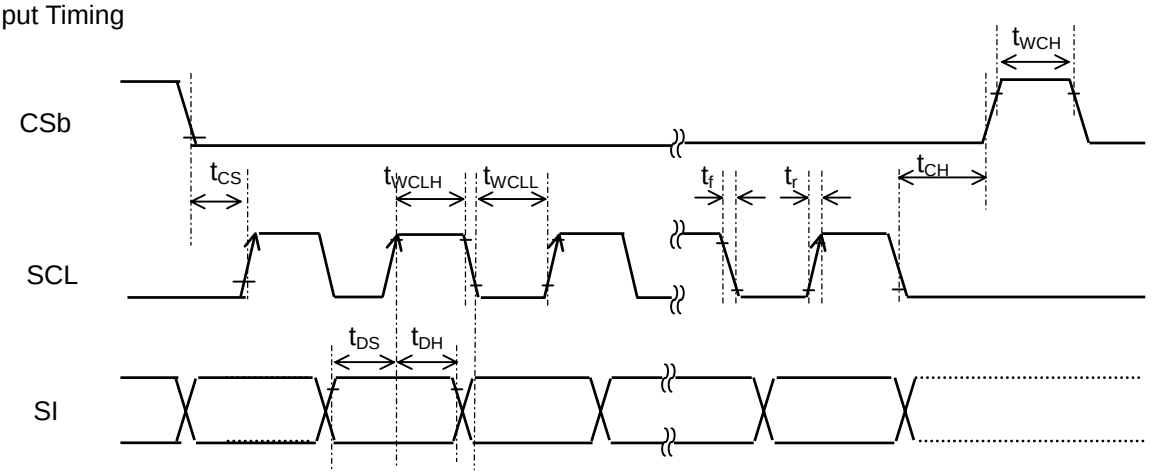


- AC characteristics

(V_{DD}=V_0=2.4 to 3.6V, V_{SS}=0V, Ta=-40 to +105°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT	Note
"L" Level Clock Pulse Width	t_{WCLL}		230	-	-	ns	
"H" Level Clock Pulse Width	t_{WCLH}		230	-	-	ns	
Data Setup Time	t_{DS}		30	-	-	ns	
Data Hold Time	t_{DH}		30	-	-	ns	
CSb Setup Time	t_{CS}		50	-	-	ns	
CSb Hold Time	t_{CH}		50	-	-	ns	
CSb"H" Level Pulse Width	t_{WCH}		250	-	-	ns	
Rising Time	t_r		-	-	20	ns	
Falling Time	t_f		-	-	20	ns	

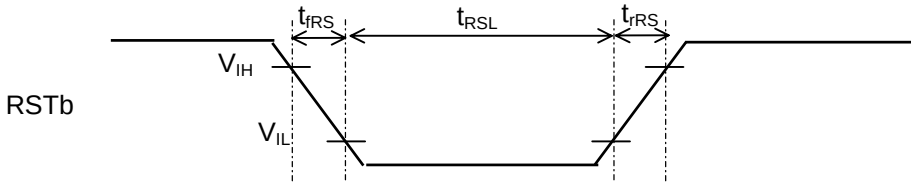
- Input Timing



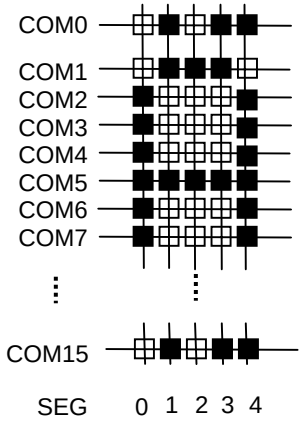
- Input condition when hardware reset circuit is used

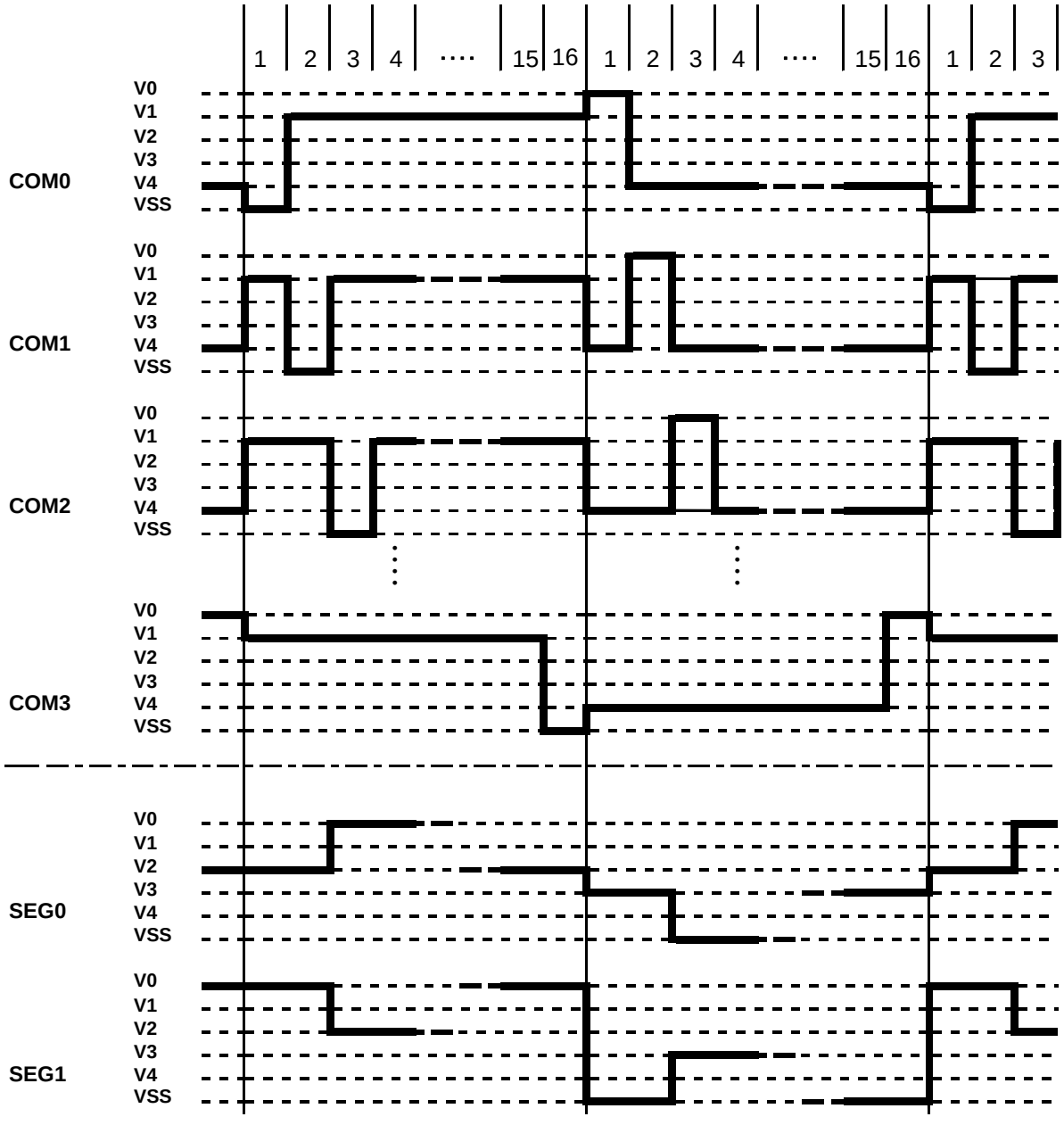
(Ta=-40 to +105°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Reset Input “L” Level Width	t_{RSL}	f_{OSC}=30.8kHz±18%	1.3	-	-	ms
		f_{OSC}=184.8kHz±18%	0.3	-	-	ms
Reset Rising Time	t_{rRS}		-	-	100	ns
Reset Falling Time	t_{fRS}		-	-	100	ns

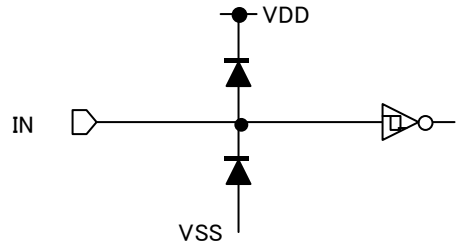


LCD Operating Wave Form

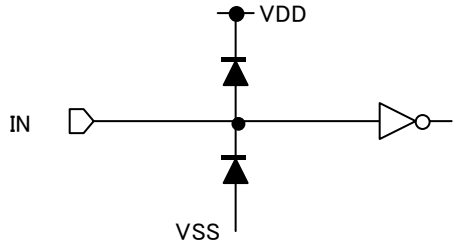




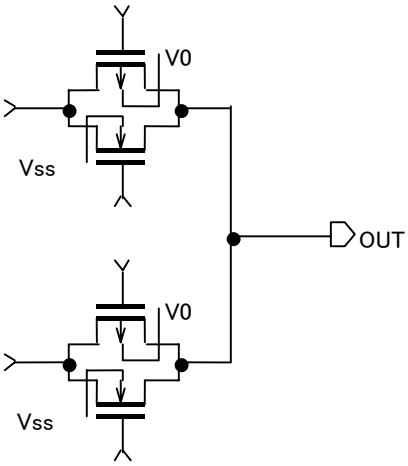
■ **Input and Output Circuit**



RSTb, CSb, SI,SCL



OSC, EXOSC, INHb, TESTIN, BOOST, TESTIN2

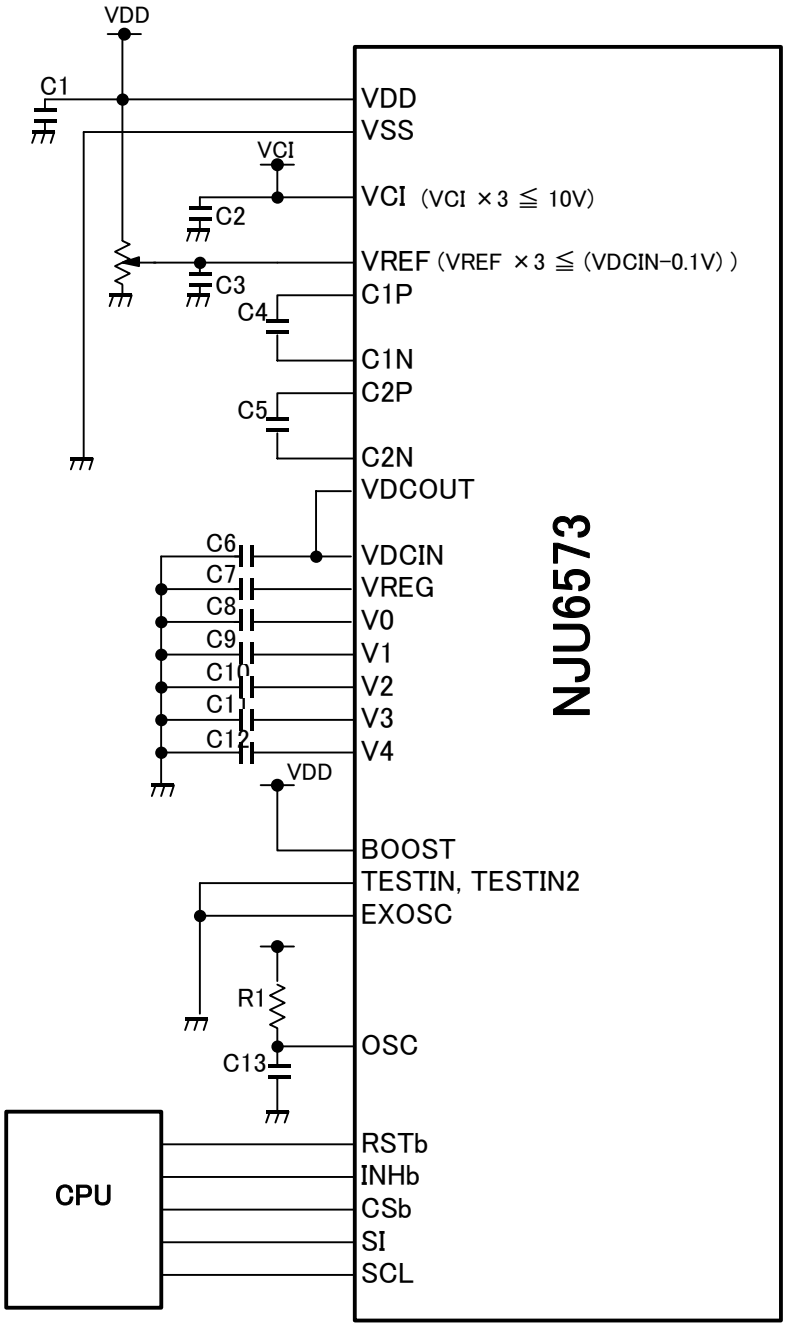


SEG0~SEG99, COM0~COM15

■ APPLICATION CIRCUIT

1)Circuit1

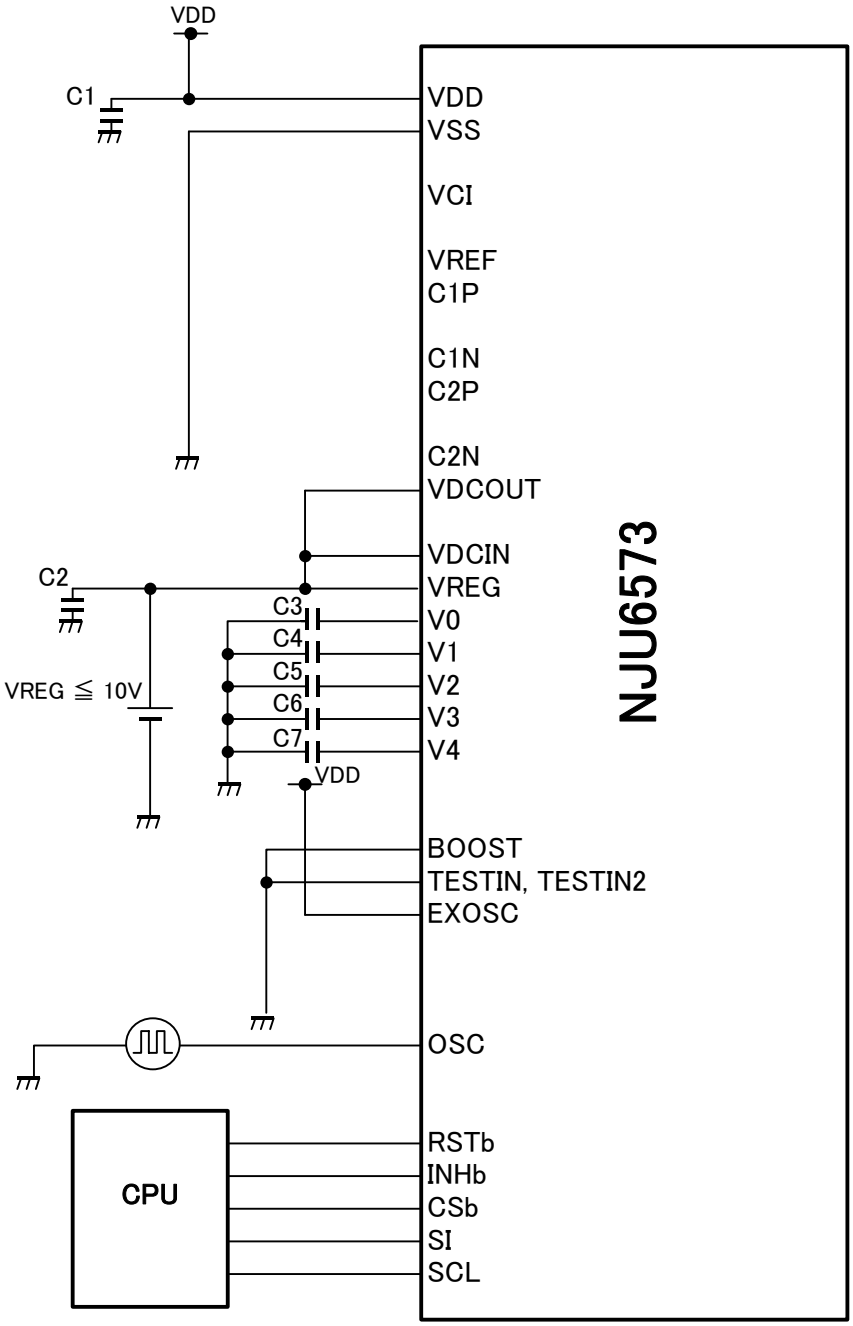
Booster ON, Internal OSC



Reference value

R1	200kΩ
C13	100pF
C4,5,6,7	1.0-4.7μF
C1-C3,C8-C12	0.1-1.0μF

2)Circuit 2
Booster OFF, Regulator OFF (External power supply mode), External OSC

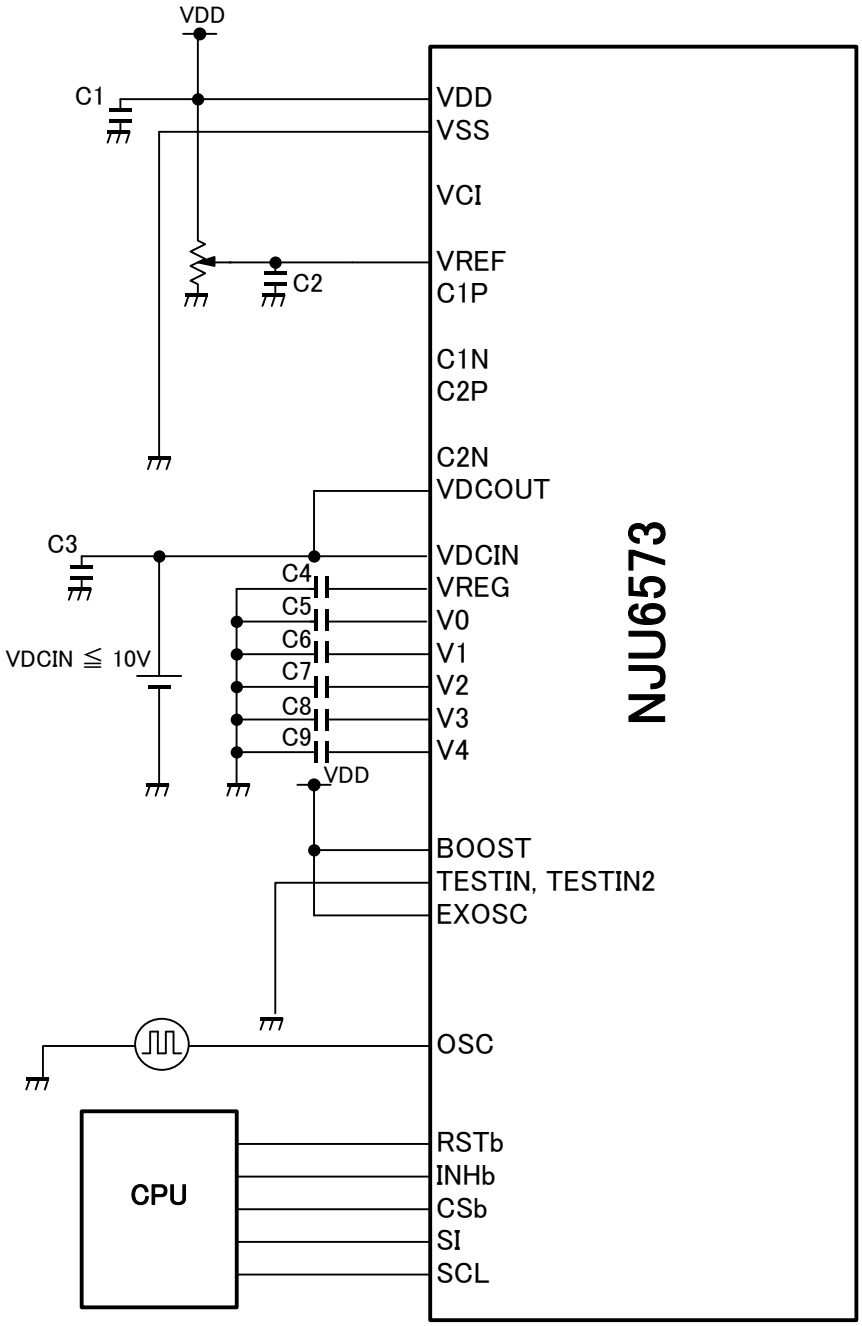


Reference value

C2	1.0-4.7μF
C1,C3-C7	0.1-1.0μF

3)Circuit3

Booster OFF, Regulator ON, External OSC



Reference value

C3,4	1.0-4.7μF
C1,C2-C9	0.1-1.0μF

[CAUTION]
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